REMARKS

Claims 1-3 and 10-23 are pending. Claims 1, 3, 12, 14, 20 and 22 are amended with this response. Reconsideration of the application is respectfully requested for at least the following reasons.

I. REJECTION OF CLAIMS 1-23 UNDER 35 U.S.C. § 112

Claims 1-23 were rejected under 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The office action specifically states that, "[d]escription of the entry, the data frames, the receive descriptor ring, the descriptor management system and the counters are vague and indefinite." The applicant respectfully requests clarification as to the specific issue of the rejection.

U.S.C. 112 states that, "[t]he test for definiteness under 35 U.S.C. 112, second paragraph, is whether 'those skilled in the art would understand what is claimed when the claim is read in light of the specification.'" MPEP 2100-212. This is read to mean that a description of terms and process used within the claims must be further clarified by the specification. In the case of the present invention, the claims provide a functional connection of terms while the specification provides further explanation. For example, claim 3 references receive descriptor rings comprising a unique priority level and one or more receive descriptors, the receive descriptors being associated with one or more data frames received from the network that are to be transferred to the host. This claim provides a functional relationship between receive descriptor rings and the receive descriptors (*i.e.*, the receive descriptor rings are comprised of receive descriptors) and relates the concept of priority to the receive descriptor ring. It further associates the descriptors with data frames and therein cumulatively describes the relationships between the receive descriptor ring, receive descriptors, data frames, and priority. The specification further explains the process by which these concepts are used beginning on page 15. It is respectfully requested that examiner provide further guidance on what the claims are lacking to fulfill the U.S.C. 112 requirement.

II. REJECTION OF CLAIMS 1, 2, AND 11 UNDER 35 U.S.C. § 102(b)

Independent claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,724,358 (Headrick et al.). Withdrawal of the rejection is respectfully requested for at least the following reason.

Claim 1 of the present invention relates to a method of transferring data between a host and a network, wherein one or more receive descriptors in one of a plurality of receive descriptor rings comprising the data transfer queues point to the data stored in a memory buffer and wherein the data contains the same content as the data received from the network.

As will be argued below, Headrick et al. does not anticipate the present invention because Headrick et al. teach pointers stored in pointer memory pointing to ***data located in queues***, while the present invention claims queues comprising receive descriptors which ***point to data not located in the queues***.

In the abstract, Headrick et al. teach "pointers to buffer locations containing data packets having a particular priority level stored in one or more priority sub-queues" (abstract, line 9-11). The specification further explains what this means. The node 22 receives the data and the routing and buffering unit 126 stores the data with an internal tag (col. 6, line 1-2). For outputting data, data stored in the routing and buffering unit 126 is ***mapped directly to each output queue element*** (col. 9, line 47-49) contained in the pointer memory 178,180 (col. 8, line 65). Each data entry further has a next memory location field 294. The output queue has a pointer memory associated with it (col. 9, line 49-50) which points with a head pointer to a memory location within the output queue. That memory location will be transferred and will also point to the location of the next memory location field. This process will repeat until the tail pointer is reached, at which time the pointer memory will advance to the next head pointer/priority level of the pointer memory (fig. 11). In this manner data is transferred from its mapped to location in the queues located in the buffer memory.

This is different than claim 1 of the present invention, wherein the data queues are comprised of receive descriptors which ***point to data stored in a buffer memory.***

The queues have associated with them a particular priority level. In general, the highest priority level queue will output first. This queue will output data associated with the individual receive descriptors in the particular receive descriptor ring(s) associated with the queue. In contrast to Headrick et al., ***the queue of the present invention points to data packets separate from the queue. There is no mapping of data from the buffer memory to the queue***. Therefore, there is no need for pointer memory outside of the queue as required in Headrick et al. Since Headrick et al. fail to teach receive descriptors located in the data queues pointing to data stored outside the queue they fail to anticipate claim 1 of the present invention.

Independent claim 1 was rejected as being anticipated by Headrick et al. Claims 2 and 11 depend upon claim 1, respectively, and add further limitations thereto. The primary reference does not teach or suggest the present inventions of claim 1. Therefore claims 2 and 11 are also not anticipated by the cited art. Accordingly, withdrawal of the rejection is respectfully requested.

III. REJECTION OF CLAIMS 12, 13, 20, AND 21 UNDER 35 U.S.C. § 102(b)

Independent claims 12 and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,724,358 (Headrick et al.). Withdrawal of the rejection is respectfully requested for at least the following reasons.

Claim 12 of the present invention relates to a system for transferring data between a host and a network using a shared memory comprising a plurality of data transfer queues in a shared memory and a network interface system comprising a descriptor management system storing a plurality of priority levels, the priority levels being individually associated with one of the data transfer queues, wherein one or more receive descriptors in one of a plurality of receive descriptor rings comprising the data transfer queues point to the data stored in a memory buffer and wherein the data contains the same content as the data received from the network.

Claim 20 of the present invention relates to a network interface system comprising a descriptor management system storing a plurality of priority levels, the

priority levels being individually associated with a data transfer queue in a shared memory, wherein one or more receive descriptors in one of a plurality of receive descriptor rings comprising the data transfer queues point to the data stored in a memory buffer and wherein the data contains the same content as the data received from the network.

As stated above, Headrick et al. fail to teach one or more receive descriptors in a receive descriptor ring comprising the data transfer queues pointing to the data stored in a memory buffer outside the queue.

Further, in figure 1, Headrick et al. show a block diagram of an asynchronous transfer mode (ATM) communication system. The ATM communication system comprises a number of nodes 22 interconnected by communication links 42. Headrick et al. state that a node may include a plurality of input modules 80, a switch fabric 82 and a plurality of output modules (col. 4, line 20-21). Figure 5 shows a switch fabric 82 in more detail. The switch fabric of figure 5 comprises a router and buffering unit 126, a buffer manager 128, an input layer 122 and input translation 124, and an output layer 132 and output translation 134. Figure 7 shows the router and buffering unit 126 and buffer manager 128 in more detail. The buffer manager comprises pointer memory 178 and 180. Headrick et al. teach that output queues are stored in the pointer memories 178, 180 and further that sub-queues may be present ***within*** the overall output queue (*i.e.,* sub-queues are stored in the pointer memories also) (col. 9, line 56-58).

The network interface periphery as claimed in claims 1, 12, and 20 of the present invention comprises a descriptor management system storing a plurality of priority levels, the priority levels being individually associated with one of the data transfer queues. Headrick et al. teach that a combination of the output queue and the pointer memory determine the priority level and that sub-queues are used for multiple priority levels (col. 9, line 50-58). Queues, sub-queues are stored in pointer memories 178, 180 located in the buffer manager 128 (col. 8., line 61-65, col. 9, line 56-58). Headrick et al. do not teach any other storage of queues or sub-queues. Therefore, ***for Headrick et al. to teach a network interface periphery it must comprise the buffer***

manager 128 since it is necessary that it include the pointer memories 178, 180 which store the queues and sub-queues as taught by claims 1, 12, and 20.

The shared memory of claims 1, 12, and 20 of the present invention comprises data transfer queues. As previously stated, Headrick et al. teach that the pointer memories 178, 180 contain a plurality of linked list type data structures that ***are the output queues*** for the plurality of output ports. Therefore, for Headrick et al. to teach a shared memory comprising data transfer queues ***it is necessary that the shared memory also comprise the buffer manager 128*** (which comprises the pointer memories 178,180 which comprises the queues).

For Headrick et al. to anticipate the present invention: (1) the structure analogous to the network interface must consist of the buffer manager 128 so that the network interface contains a plurality of priority levels; and (2) the structure analogous to the shared memory must consist of the buffer manager 128 so that the shared memory contains the data queues. ***Since the shared memory and the network interface periphery are separate objects it is not possible that both comprise the buffer manager 128 as would be necessary for Headrick et al. to anticipate the present invention.*** Therefore, Headrick et al. do not anticipate the shared memory and network interface periphery as taught in claims 1, 12, and 20 of the present invention.

Independent claims 12 and 20 were rejected as being anticipated by Headrick et al. Claim 13 depends upon claim 12 and adds further limitations thereto. Claim 21 depends upon claim 20 and adds further limitations thereto. The primary reference does not teach or suggest the present inventions of claims 12 or 20. Therefore claims 13 and 21 are also not anticipated by the cited art. Accordingly, withdrawal of the rejection is respectfully requested.

IV. REJECTION OF CLAIMS 3, 14, 22, AND 15 UNDER 35 U.S.C. § 103(a)

Claims 3, 14, 15, and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,724,358 (Headrick et al.). Withdrawal of the rejection is respectfully requested for at least the following reasons.

As stated above, Headrick et al. do not teach or suggest the invention of independent claims 1, 12, or 20. Claim 3 depends upon claim 1, and adds further limitations thereto. Claim 14 and 15 depend upon claim 12 and add further limitations thereto. Claim 22 depends upon claim 20 and adds further limitations thereto. Because the primary references do not teach the present invention of claims 1, 12, or 20, claims 3, 14, 15, and 22 are also non-obvious over the cited art. Accordingly, withdrawal of the rejection is respectfully requested.

V. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP762USWOUS.

Respectfully submitted,
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